CLAIMS

1. Very wide band amplifier circuit including a distributed amplification cell (100) connected to a biasing cell (200), the amplification cell (100) including several transistors (T1) connected in parallel between a drain line and a grid line, each terminated at one of its ends by a load (Zin, Zout), the biasing cell (200) including at least one transistor (T2) connected between a power source (V_{DD}) and the drain line of the amplification cell (100), said biasing cell having an overall impedance equal to the impedance of the load (Zout) connected to the end of the drain line of the amplification cell (100), characterized in that the grid (G2) of the transistor (T2) of the biasing cell (200) is connected to the node (201) of a divider bridge (R1R2, R1T3) so as to set its grid (G2) potential (V_{G2}), and in that the grid (G2) and the source (S2) of said transistor (T2) are connected together by means of at least one capacitor (C1, C2).

2. Amplifier circuit as claimed in claim 1, characterized in that it includes a resistor (R) mounted in series with the capacitor (C) between the grid (G2) and the source (S2) of the transistor (T2) of the biasing cell (200).

3. Amplifier circuit as claimed in one of the preceding claims, characterized in that it includes a resistor (R3) connected between the grid (G2) of the transistor (T2) and the node (201) of the divider bridge (R1R2, R1T3).

4. Amplifier circuit as claimed in one of the preceding claims, characterized in that the divider bridge (R1T3) includes at least one transistor (T3).

5. Amplifier circuit as claimed in one of the preceding claims, characterized in that the biasing cell (200) includes several transistors (T2) arranged in parallel and several divider bridges (R1R2) arranged in parallel and in that each of the transistors (T2) is connected by its grid (G2) to one of the divider bridges (R1R2).

6. Amplifier circuit as claimed in one of the preceding claims, characterized in that it includes as least one resistor (R5) mounted in parallel with the biasing cell (200).

7. Amplifier circuit as claimed in one of the preceding claims, characterized in that it includes at least one resistor (R6) mounted in series with the biasing cell (200).

8. Amplifier circuit as claimed in one of the preceding claims, characterized in that it includes an inductor (L7) and a resistor (R7) arranged in parallel, mounted in series with the biasing cell (200).

9. Amplifier circuit as claimed in one of the preceding claims, characterized in that it includes at least one resistor (R8) and one capacitor (C8) arranged in series, connected between the drain (D2) of the transistor (T2) and the ground.

10. Biasing cell (200) for amplifier circuit, characterized in that it includes at least one transistor (T2) designed to be connected between a power supply (V_{DD}) and a drain line of an amplification cell (100), characterized in that the grid (G2) of the transistor (T2)

of the biasing cell (200) is connected to the node (201) of a divider bridge (R1R2, R1T3) so as to set its grid (G2) potential (V_{G2}), and in that the grid (G2) and the source (S2) of said transistor (T2) are connected together by means of at least one capacitor (C1, C2).